SAMPLE-AND-HOLD PHASE SHIFTER CONTROL VOLTAGE DISTRIBUTION IN A PHASED ARRAY UTILIZING VOLTAGE-PROPORTIONAL PHASE SHIFT DEVICES

FIELD OF THE INVENTION

[0001] The present invention relates in general to communication systems and subsystems thereof, and is particularly directed to a phased array architecture, comprised of a plurality of analog voltage-proportional phase shift elements and a sample-and-hold control voltage distribution network coupled thereto. The sample-and-hold control voltage distribution network selectively couples the voltage output of a digital-to-analog converter to the control voltage input of one or more voltage-controlled phase shift elements that make up the phased array architecture, thereby producing whatever phase shift pattern is desired.

BACKGROUND OF THE INVENTION

[0002] In the course of development of communication systems and networks that operate at ever increasing frequencies (e.g., on the order of 1-50 GHz and above), the electronics industry continues to look for ways to decrease the cost of components of which such systems and networks are comprised. Because beam steerable and agile systems customarily employ phase shift components, their feed and control interconnect architecture layouts can be quite complex and costly to deploy. Thus, there is currently a need for low cost and reduced complexity phase shift architectures that are capable of operating and relatively high frequencies.

SUMMARY OF THE INVENTION

[0003] In accordance with the present invention advantage is taken of analog voltage-proportional phase shift components to implement a relatively low cost analog phased array architecture, that is configured to selectively couple the voltage output of a digital-to-analog converter to the voltage control input of one or more voltage-controlled phase shift elements that make up the phased array architecture, thereby producing whatever phase shift pattern is desired.

[0004] As will be described, the invention is configured of a spatially distributed array of voltage-controlled analog phase shift elements, such as tunable varactor components, dielectric elements or paraelectric components, such as ferro-electric devices. Each phase

shift element has an input port to which a respective input signal is supplied, and an output port from which a phase-shifted output signal is obtained. The phase of the output signal is shifted in phase relative to the phase of the input signal in accordance with a control voltage supplied to a voltage control port thereof. Control voltages for defining the phase shift through each phase shift element are derived from a multiple analog voltage supply unit, configured as series of sample-and-hold switches that are selectively coupled to the output of a digital-to-analog converter.

[0005] In operation, all of the switches of the switching units are initially in their default open state. In order to impart a phase shift control voltage to one or more phase shift elements of the array, a control unit supplies a prescribed combination of a digital control code to the digital-to-analog converter and a switch control code to the sample-and-hold switches. The digital control code supplied to the digital-to-analog converter defines the magnitude of the control voltage and thereby the magnitude of phase shift to be produced by one or more phase shift elements to which that voltage is supplied by one or more of the switching units.

[0006] This also allows the control unit to compensate for non-linearities in any phase shift device. The switch control code supplied to the switching units specifies one or more of the phase shift elements to be programmed with the analog voltage output by the

digital-to-analog converter. Once a respective programming voltage has been supplied to a phase shift element its associated switch within a respective switching unit is opened, to complete the hold condition for the phase shift element.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The single Figure diagrammatically illustrates an embodiment of an analog voltage-proportional phase array architecture according to the present invention.

DETAILED DESCRIPTION

[0008] Before describing in detail the phased array architecture of the present invention, it should be observed that the invention resides primarily in a modular arrangement of conventional communication circuits and components and an attendant supervisory controller, that controls the operations of such circuits and components. In a practical implementation that facilitates their being packaged in a hardware-efficient equipment configuration, this modular arrangement may be implemented by means of analog voltage-proportional phase shift elements and an associated application specific integrated circuit (ASIC) chip set.

[0009] Consequently, the architecture of such arrangement of circuits and components has been illustrated in the drawings by a readily understandable block diagram, which shows only those specific details

that are pertinent to the present invention, so as not to obscure the disclosure with details which will be readily apparent to those skilled in the art having the benefit of the description herein. Thus, the block diagram illustration is primarily intended to show the major components of the invention in a convenient functional grouping, whereby the present invention may be more readily understood.

[00010] Attention is now directed to the single Figure, which diagrammatically illustrates an embodiment of an analog voltage-driven phase array architecture according to the invention. As shown therein, the phased array proper comprises a spatially distributed arrangement 10 of respective sets 10-1, 10-2, ..., 10-N of voltage-controlled analog phase shift elements 11, comprised of voltage-proportional devices, as referenced above. As a non-limiting example, a respective set 10 of phase shift elements may comprise eight phase shift elements, as shown.

[00011] Within an individual set of voltage-proportional phase shift elements, each phase shift element 11 has an RF input port 12, to which a respective input signal is supplied, and an RF output port 13 from which a phase-shifted output signal, that is shifted in phase relative to the input signal in accordance with a control voltage supplied to an analog control voltage input 14 thereof, is obtained. Control voltages for defining the magnitude of phase shift through the various phase shift elements are derived from an associated sample-and-hold switching

unit 20, containing N controlled switches 20-1 through 20-N, where N=8 in the present example. Inputs 21 of the individual sample-and-hold switches of each of the switching units 20 are connected in common to the output of a digital-to-analog converter (DAC) 30, while outputs 22 thereof are coupled to respective ones of their associated set of phase shift elements. Each switching unit 20 is further coupled via a switch control bus 23 to a supervisory control unit 40, which is operative to define the phase shift pattern that is loaded into the phase shift elements of the array, as well as the digital input to the DAC.

[00012] The analog voltage-driven phase array architecture of the invention operates as follows. Initially all of the switches of the switching units are in their default open state, as shown. In order to impart a phase shift control voltage to one or more phase shift elements of the array, control unit 40 supplies a prescribed combination of a digital control code to the DAC 30 and a switch control code to the switching units 20. The digital control code supplied to the DAC 30 serves to define the magnitude of the control voltage delivered by the DAC and thereby the magnitude of phase shift to be produced by one or more phase shift elements to which that voltage is supplied by one or more of the switching units 20. This also allows the control unit 40 to compensate for non-linearities in any phase shift device. The switch control code supplied to the switching units 20 serves to specify which one or

more of the phase shift elements is to be programmed with the analog voltage output by the DAC. Regardless of the programming scheme employed, once a respective programming voltage has been supplied to a phase shift element 11, its associated switch within a respective switching unit 20 is opened, to complete the hold condition for the phase shift element.

[00013] As a non-limiting example, the individual switches of the switching units may be closed one at a time (e.g., sequentially) and, with each switch closure, a control code supplied to the DAC so as to program that switch's associated phase shift element 11 with the phase shift produced by the analog voltage output by the DAC. As a more efficient programming routine, the DAC may be controlled so as to sequentially step through a series of codes that are effective to produce a ramp voltage at the output of the DAC. During this ramping of the DAC voltage, switch closure codes are produced on the control bus 23, so that one or more phase shift elements are supplied with the appropriate voltage produced by the DAC.

[00014] As an adjunct to the embodiment described above, auxiliary storage capacitors, one of which is shown in broken lines 15, may be employed to augment the holding voltage functionality of the phase shift elements. In addition, voltage follower circuits, such as that shown in broken lines 16, may be coupled with the inputs 21 to the sample-and-hold switching units 20 to extend the

number of phase shift elements that may be driven by the DAC.

[00015] While we have shown and described an embodiment in accordance with the present invention, it is to be understood that the same is not limited thereto but is susceptible to numerous changes and modifications as known to a person skilled in the art. We therefore do not wish to be limited to the details shown and described herein, but intend to cover all such changes and modifications as are obvious to one of ordinary skill in the art.